# 7 TOLL SYSTEMS T1C/T1 QUASI RANDOM SIGNAL SOURCE (QRSS)

CHANGES

D. Description of Changes

D.1 Since this is a preproduction change, no record of changes will be made at this time.

BELL TELEPHONE LABORATORIES, INCORPORATED

DEPT 4223-BBG-JBS

# TOLL SYSTEMS
# T1C/T1 QUASI-RANDOM SIGNAL SOURCE
# (QRSS)

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## SECTION I - GENERAL DESCRIPTION

### 1. PURPOSE OF CIRCUIT

1.01 This circuit provides up to 50 T1 or T1C quasi-random signals to 100-ohm loads. The signal fullfills the following needs for T1C or T1 Systems.

(a) Provides an error-free signal during troubleshooting routines.

(b) Drives maintenance spare lines through bridging repeaters.

(c) Drives multispan spare lines.

(d) Drives idle lines during system turn-up.

(e) Provides a far-end source with a known sequence for bit-error rate measurements.

### 2. GENERAL METHOD OF OPERATION

2.01 The outputs are available in two groups of 25 each. Each group can either be T1C or T1 type, depending on whether ED-3C569-( ), Group 1 or Group 2 assembly has been chosen for the corresponding signal source plug-in.

2.02 The circuit is contained in a 1-3/4 inch high panel. It can be mounted in a 23-inch wide bay with holes for either 1-3/4 inch type panels or 2-inch type panels. It consists of a power and alarm plug-in and slots for two signal source plug-ins. The circuit requires -48 volt power.

2.03 The power and alarm plug-in ED-3C568-( ) provides a fuse for the incoming power and also generates +5 volts power through a dc-to-dc converter for use by logic circuits. It provides relay contact closures for initiating central office audio and visual alarms in case a failure is detected in the unit.

2.04 The T1C signal source ED-3C569-( ), Group 1, is a plug-in unit. It contains a 20-bit shift register with exclusive-or feedback to generate a digital word with a period of 1,048,575. The digital word is fed to nine output stages. Eight output stages drive a total of 24 100-ohm loads. The ninth output stage drives the 25th 100-ohm load at the rear of the unit and the load connected to the source jack located on the front panel.

2.05 The T1 signal source ED-3C569-( ), Group 2, is also a plug-in. Its output contains a digital word with a period of 1,048,575 which is stuffed to contain no more than 14 consecutive zeros. The output signal contains overshoot per T1 System requirements. The signal is identical to that from J98710R except for the overshoot and resistive isolation among the outputs.

2.06 There are fifty 100-ohm resistors located at the back of the unit to serve as dummy loads. When a system is connected to a particular output, the 100-ohm resistor corresponding to that output must be disconnected.

SECTION II - DETAILED DESCRIPTION

1. POWER AND ALARM PLUG-IN - ED-3C568-( )

1.01 FS 1 on the SD shows interconnection between ED-3C568-( ) and other parts of the circuit. Major blocks of the ED assembly are shown in CD Fig. 1. A more detailed description corresponding to CPS 1 follows.

1.02 The dc-to-dc converter A1 converts incoming -48 volt power to 5 volts for powering logic circuits. The alarms from either of the signal source plug-in units or a blown fuse activate relay K1 whose contacts on pairs 1,2; 3,4; 5,6 close for driving central office audio and visual alarms. The relay can be deactivated and the contacts opened by depressing the alarm cut-off (ACO) pushbutton momentarily. While the ACO feature is in operation, the ACO indicator light-emitting diode (LED) is on. As soon as the plug-in responsible for alarm or the blown fuse is corrected or removed, the alarm latch and ACO light reset automatically.

1.03 When the fuse blows, the auxiliary lead in fuse holder gets shorted to incoming -48 volts. A current path through CR1, R6, K1, CR4, DS2 is established, activating the relay and lighting FUSE indicator.

1.04 Alarm conditions on the signal source plug-ins input a logic zero on pin 14 or 15, which in turn cause a logic zero at the output of IC1A, turning on Q1 and Q2 to establish a current path through CR1, R6, K1, CR3, and Q2. The Q output of IC2A is normally at logic one. R1 and R2 supply a logic one to pins 14 and 15 to avoid indication of an alarm in case either of the two signal source plug-ins is removed. C3 and C4 reduce the effects of transients when the plug-in units are removed or inserted into the chassis. Depressing ACO presents a rising waveform to clock input of IC2A and changes its Q output to a logic zero, causing output of IC1A to go back to a logic one. The voltage drop across RV1 prevents Q1 from remaining on when IC1A output is at logic one. Thus, base of Q2 is starved and the low impedance current path through K1 is broken. Now, ACO is in operation and logic one at Q output of IC2A turns on the ACO indicator DS1. As soon as the alarming plug-in(s) are removed or corrected, pins 14 and 15 go to logic one causing output of IC1B to go to logic zero which causes IC2A to preset its $\overline{Q}$ output to logic one. The $\overline{Q}$ output of IC2A goes to logic zero and the ACO indicator resets to an off condition.

2. T1C AND T1 SIGNAL SOURCES - ED-3C569-(), GROUP 1 AND GROUP 2, RESPECTIVELY

2.01 A block diagram, CD Fig. 2, shows the principal components of the CD assembly. The crystal oscillator at T1C (3.152 MHz) or T1 (1.544 MHz) symbol rate clocks the 20-bit shift register to generate a quasi-random digital word with a period of $2^{20} - 1 = 1,048,575$. The all zero lock up detector and restarter feeds a logic one at the input in case the shift register gets stuck in an all zero mode. Nineteen consecutive zeros appear only once in the digital word and a synchronizing pulse is generated when they occur. In the case of T1, the leading zeros are stuffed with logic ones in cases when more than 14 consecutive zeros are present in the logic word. The logic word is applied to the polarity converter which alternates the ones to produce a bipolar signal at the outputs. An alarm is generated whenever the transitions at the output of polarity converter stop. The overload sensor senses the supply current to the output stages and logically switches it off in the case of overload. A more detailed description of CPS 2 and CPS 3 follows.

2.02 IC2, IC3, IC14 comprise the 20-bit shift register which shifts on rising edge of the clock (last four bits on IC14 are not used). Normally, pin 11 of IC7 is a zero; hence, IC7C and IC7D comprise exclusive-or feedback from 17th and 20th bit to the input.

2.03 The sixth bit output goes through inverter IC8D to drive IC9 and IC10A which help accomplish the functions of all zero lock up detector, synchronizing pulse, 14 zeros detector, and pulse stuffer. The timing diagram of CD Fig. 3 illustrates these functions for the case when 19 consecutive zeros appear in the word. When the sixth bit is a logic one, the following rising edge on clock loads the counter IC9 to 0010 (or decimal 2). The counter will advance on each succeeding zero until another logic one appears on sixth bit output. Row 3 in CD Fig. 3 shows the state of the counter. At the end of 14 consecutive zeros, the carry output clocks IC10A output to logic one which, in turn, stuffs ones into IC8C for the case of T1 signal source. The 20th bit output, which is shifted by 14 clock pulses from sixth bit is shown in row six. The stuffed output on IC7A is shown in the next row.

2.04 When 19 consecutive zeros pass by the sixth bit, logic one on IC10A output and Qc on IC9 are combined by IC11A to give a synchronizing pulse. The synchronizing pulse is further shaped by the clock signal through IC12B to eliminate spikes that may occur at IC11A output due to differences in transition times of various devices. In case the shift register is stuck in an all zero mode, Q on IC9 and IC10 output will go to logic one after 22 zeros and a logic one will be generated at IC6A output which will insert a logic one at the shift register input.

2.05 The bipolar converter and the alarm functions are illustrated in the timing diagram of CD Fig. 4. IC7B, IC8A, IC10B, and IC11B and C accomplish the bipolar converter function and IC4,IC5 accomplish the alarm function. As row 5 shows, a pulse is generated at IC8A output each time the word is a logic one. This clock pulse toggles IC10B whose outputs alternate pulse occurrences on IC11B and C outputs, thus performing the bipolar converter function. IC4 is preset to a logic one by pulse from IC11B and clocked to a logic zero by pulse from IC11C. If either of the IC11B or IC11C outputs fail, the IC4 output will maintain a static output and IC5 will not be triggered, causing the alarm lead on pin 1 to go to logic zero.

2.06 IC15 senses the current to the output stages. Normally IC15 output is at logic zero, however, when the current exceeds a threshold determined by the setting on R53, the IC15 output goes to a logic zero causing the output stages to turn off. The time loonstant for charging C38 is much longer than that for C37, which keeps the output stages off when the power is initially turned on. Thus, the magnitude of initial inrush currents is kept low.

2.07 IC1F is needed as a buffer between the oscillator and the various loads. Because the 105 oscillator output has a longer (high) than 50-percent duty cycle, IC1D is used in series with IC1F so that the output pulses shall not be too long to meet the requirements.

2.08 There are nine output stages. Each stage generates an open circuit 9 volts peak-to-peak signal. About half of the signal is dropped across a pair of 27-ohm isolation resistors. Each output stage drives the equivalent of three 154-ohm loads each. The auxiliary windings on the output transformers have an inductor-resistor network in case of T1 signal source to provide pulse overshoot. Each stage must be terminated into three loads to maintain proper overshoot amplitude and fall time (termination resistors which are clipped after connection to office loads are made on ED-3C589-( )). The termination or loading resistors are not necessary for T1C signal source board.

3. T1C/T1 ORSS INTERFACE BOARD - ED-3C589-( )

3.01 This board contains loading resistors for the signal sources. In order to provide front panel interchangeability between T1C and T1 sources, the same interface board is used for both types of sources even though the loading resistors are not needed for T1C source.

3.02 Ground, Vcc, and -48 volts are wired to this board from the power and alarm board. At present, -48 volts is not used by the ED-3C569-( ), Issue 1, but is available for use by future plug-ins.

SECTION III - REFERENCE DATA

1. WORKING LIMITS

1.01 The power input can vary between -42 and -54 volts. The output pulse amplitude may be below 6 volts peak-to-peak at -42 volts input.

2. FUNCTIONAL DESIGNATIONS

2.01 FUSE: Whenever the fuse blows, the red LED indicator lights and the alarm relay is activated to drive central office audio and visual alarms. If the blown fuse is removed, the relay deactivates and the alarms stop.

2.02 ACO: When either of the source plug-ins alarms, the relay is activated to drive central office audio and visual alarms. Depressing the ACO pushbutton switch momentarily will light the ACO indicator and deactivate the relay. If the alarming plug-in becomes good, or it is removed from the unit, the ACO indicator will go off and the alarming logic will reset itself.

2.03 MON: This jack provides approximately a 600-millivolt peak-to-peak signal into 100 ohms across tip and ring.

2.04 SOURCE: This jack provides approximately a 6-volt peak-to-peak signal into 100 ohms across tip and ring.

2.05 SYNC: An approximately 3-volt peak-capacitor coupled pulse is provided once per period. For T1 source, the frequency of the synchronizing pulse is approximately 1.47 Hz and for T1C source, it is 3.00 Hz.

2.06 ALM: The alarm indicator lights whenever the transitions on either of the two rails at the bipolar converter output cease. An alarm output also drives the power and alarm plug-in to activate the alarm relay.

3. FUNCTIONS

3.01 This circuit provides up to 50 T1 or T1C quasi-random signals of 6 volts peak-to-peak amplitude. The sequence at T1 rate is stuffed to contain no more than 14 consecutive zeros while the sequence at T1C rate may contain up to 19 consecutive zeros.

4. CONNECTING CIRCUITS

4.01 T1C/T1 Office Repeater Bay - SD-3C252-01

4.02 Digital Transmission Facilities - Patch and Cross Connect Interconnection Circuit (DSX1, DSX1C, DSX2) - SD-99503-01

5. MANUFACTURING TESTING REQUIREMENTS

5.01 Manufacturing testing requirements are specified in X-78965.

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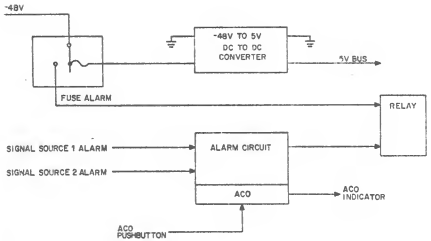
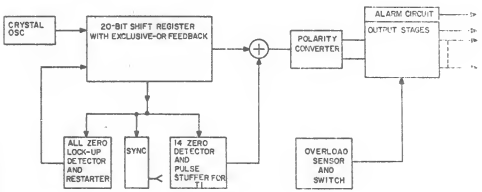
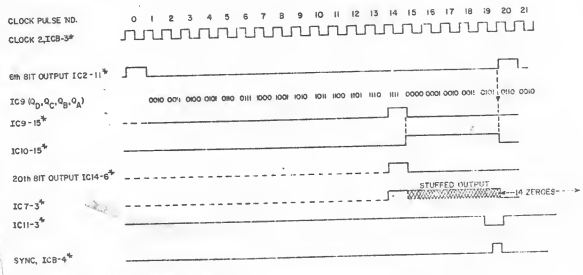
Attachments:
CD Fig. 1 thru CD Fig. 4



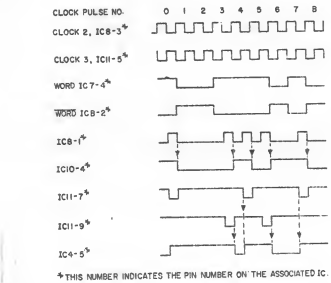

CD Fig. 1 - Block Diagram of Power and Alarm Plug-in, ED-3C568-( )




CD Fig. 2 - Block Diagram of T1C and T1 Signal Source Plug-in, ED-3C569-( ), Group 1 and Group 2




**CD Fig. 3 - Timing Diagram for ED-3C569-( ), Group 2 to Illustrate Pulse Stuffing and Sync**




**CD Fig. 4 - Timing Diagram for ED-3C569-( ), Group 1 and Group 2 to Illustrate Bipolar Converter and Alarm Functions**